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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2133	15

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/936,510	FURUTANI, SENICHI
	Examiner	Art Unit
	Dipakkumar Gandhi	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8, 13, 14*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. The foreign priority claim filed on 10/05/01 was not entered because the foreign priority claim was not filed during the time period set forth in 37 CFR 1.55(a)(1). For original applications filed under 35 U.S.C. 111(a) (other than a design application) on or after November 29, 2000, the time period is during the pendency of the application and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior foreign application. For applications that have entered national stage from an international application filed on or after November 29, 2000, after compliance with 35 U.S.C. 371, the claim for priority must be made during the pendency of the application and within the time limit set forth in the PCT and the Regulations under the PCT. See 37 CFR 1.55(a)(1)(ii). If applicant desires priority under 35 U.S.C. 119(a)-(d), (f) or 365(a) based upon a prior foreign application, applicant must file a petition for an unintentionally delayed priority claim (37 CFR 1.55(c)). The petition must be accompanied by (1) the claim (i.e., the claim required by 35 U.S.C. 119(a)-(d) and (f) and 37 CFR 1.55) for priority to the prior foreign application, unless previously submitted; (2) a surcharge under 37 CFR 1.17(t); and (3) a statement that the entire delay between the date the claim was due under 37 CFR 1.55(a)(1) and the date the claim was filed was unintentional. The Director may require additional information where there is a question whether the delay was unintentional. The petition should be addressed to: Mail Stop Petition, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-9, 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (JP 2000078030 A) in view of Min (US 5,430,767).

As per claim 1, Ito et al. teach a block interleaving apparatus comprising: a storage means to which (L X M) pieces of addresses are allocated (L,M: integers, 2 <= L,M), (abstract, detailed description, paragraph 17, Ito et al.);

an address generation means for generating addresses for writing and reading blocks, each block having (L X M) pieces of data as a unit to be subjected to block interleaving, in/from the storage means (abstract, Ito et al.);

Said address generation means comprising: a multiplication means for generating the product of α (α : integer, 2< =) and $M^{(b-x)}$ (x: integer, O <= x <= b, b: integer, O <= b), every time a block of a block number b is inputted (drawing 5, detailed description, paragraph 80-81, Ito et al.);

a first overflow processing means having a first comparison means for comparing the product obtained by the multiplication means with a comparison reference value L X M-1, and subtracting, as much as possible, the L X M-1 from the product on the basis of the result of the comparison to suppress overflow of the product, thereby outputting an address increment value REG corresponding to of the block having the block number b (drawing 5, detailed description, paragraph 81-83, Ito et al.);

an addition means for successively adding the (n-1)th (n: integer, 1 <= n <= L X M-1) address Ab(n-1) of the block having the block number b, to the address increment value REG outputted from the first overflow processing means, every time the block of the block number b is inputted, thereby successively generating the n-th address Ab(n) in the block of the block number b (drawing 3, detailed description, paragraph 50, Ito et al.);

and a second overflow processing means having a second comparison means for comparing the sum obtained by the addition means with the comparison reference value L X M-1, and subtracting, as much as possible, the LXM-1 from the sum on the basis of the result of the comparison to suppress overflow of the sum, thereby outputting an address to be; actually supplied to the storage means (detailed description, paragraph 50, Ito et al.);

wherein, when the first comparison means compares the product obtained by the multiplication with the comparison reference value L X M-1, the first comparison means employs, as a comparison reference value instead of the L X M-1, the minimum value A, which exceeds the L X M-1 and is included in the product (detailed description, paragraph 81, Ito et al.).

However Ito et al. do not explicitly teach the specific use of a control means for controlling the storage means so that the storage means switches the operation between the data writing and the data reading, by using the addresses generated by the address generation means.

Min in an analogous art teaches that the switching operation is controlled by a memory controller for controlling read and write operations in the memory (col. 4, lines 13-15, Min).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ito et al.'s patent with the teachings of Min by including an additional step of using a control means for controlling the storage means so that the storage means switches the operation between the data writing and the data reading, by using the addresses generated by the address generation means.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a control means would provide the opportunity to interleave the data by data writing and reading in the memory.

- As per claim 2, Ito et al. and Min teach the additional limitations.

Ito et al. teach a block interleaving apparatus comprising:

a storage means to which (L X M) pieces of addresses are allocated (L, M: integers, 2 <= L, M), (abstract, detailed description, paragraph 17, Ito et al.);

an address generation means for generating addresses for writing and reading blocks, each block having (L X M) pieces of data as a unit to be subjected to block interleaving, in/from the storage means (abstract, Ito et al.);

said address generation means including:

an address increment value storage means for storing an address increment value REG (b) corresponding to a block having a block number b (b: integer, 1 <= b), (detailed description, paragraph 17, Ito et al.);

a first initial value setting means for setting α (α : integer, 2< =) as an address increment value REG (0) corresponding to a block having a block number 0, in the address increment value storage means (detailed description, paragraph 17, Ito et al.);

a multiplication means for multiplying the output value REG(c) (c=b-1) from the address increment value storage means by M (detailed description, paragraph 17, Ito et al.);

a first overflow processing means having a first comparison means for comparing the product obtained by the multiplication means with a comparison reference value L X M-1, and subtracting, as much as possible, the L X M-1 from the product on the basis of the comparison result Lo perform a calculation equivalent to "α XM** (b-x) mod (LXM-1)" (M** (b-x) means $M^{(b-x)}$, mod is the remainder, x is an integer, O <= x <= b), thereby suppressing overflow, and outputting the calculation result as an address increment value REG(b) corresponding to the block of the block number b to the address increment value storage means (drawing 5, detailed description, paragraph 81-83, Ito et al.).

The examiner would like to point out that the calculation of "modulo" in claim 2 corresponds to the calculation of "comparison and subtraction" in the Ito et al. reference.

Ito et al. teach an address storage means for storing the n-th (n: integer, 1 <= n <= LX M-1) address Ab (n) in the block of the block number b (b: integer, 1 <= b), and outputting it to an address input terminal of the storage means (detailed description, paragraph 20, Ito et al.);

a second initial value setting means for setting the 0th address Ab (0) corresponding to the block of the block number b in the address storage means (detailed description, paragraph 21, Ito et al.);

an addition means for adding the address increment value REG (b) from the address increment value storage means, to the output value Ab (p) (p=n-1) from the address storage means (detailed description, paragraph 22, Ito et al.);

a second overflow processing means having a second comparison means for comparing the sum obtained by the addition means with the comparison reference value L X M-1, and subtracting, as much as possible, the LX M-1 from the sum on the basis of the comparison result to perform a calculation equivalent to "(Ab (n-1) + α X M** (b-x)) mod (LXM-1) ", thereby suppressing overflow of the sum, and outputting the calculation result as the n-th address Ab (n) of the block having the block number b to the address storage means (detailed description, paragraph 50, Ito et al.);

wherein, when the first comparison means compares the product obtained by the multiplication with the comparison reference value L X M-1, the first comparison means employs, as a comparison reference value instead of the L X M-1, the minimum value A, which exceeds the L X M-1 and is included in the product (detailed description, paragraph 81, Ito et al.).

Min teaches a control means for controlling the storage means so that the storage means switches the operation between the data writing and the data reading, by using the addresses generated by the address generation means (col. 4, lines 13-15, Min).

- As per claim 3, Ito et al. and Min teach the additional limitations.

Ito et al. teach the block interleaving apparatus wherein, said first initial value setting means comprises: a first constant generation means for generating the α (detailed description, paragraph 34, Ito et al.); and a first selector for selecting the α from the first constant generation means when a reset signal is inputted, and outputting it to the address increment value storage means (detailed description, paragraph 35, Ito et al.);

said first overflow processing means comprises:

a second selector for receiving the output of the multiplication means and the output of the address increment value storage means, and selecting the output of the multiplication means at the beginning of each block and selecting the output of the address increment value storage means during a period of time other than the beginning of the block (detailed description, paragraph 80-83, Ito et al.);

a first comparison means for comparing the output of the second selector with the comparison reference value A; first subtraction means for subtracting the L x M-1 from the output of the second selector (detailed description, paragraph 80-83, Ito et al.);

and a third selector for receiving the output of the second selector and the output of the first subtraction means, and selecting the output of the first subtraction means when the output of the second selector is equal to or larger than the comparison reference value, and selecting the output of the second selector when the output of the second selector is smaller than the comparison reference value; wherein the output of the third selector is supplied to the address increment value storage means through the first selector during a period of time when the reset signal is not inputted (detailed description, paragraph 41, 50, 81, Ito et al.).

- As per claim 4, Ito et al. and Min teach the additional limitations.

Ito et al. teach the block interleaving apparatus wherein said first comparison means employs, as a comparison reference value instead of the minimum value A exceeding the L X M-1, a value B, which satisfies L X M-1<B<A and it selected so that the number of logic gates constituting the comparison means is minimized (detailed description, paragraph 81, Ito et al.).

- As per claim 5, Ito et al. and Min teach the additional limitations.

Ito et al. teach the block interleaving apparatus wherein, said second initial value setting means comprises: a second constant generation means for generating a value 0 (detailed description, paragraph 18, Ito et al.);

and a fourth selector for selecting the value 0 from the second constant generation means when a reset signal is inputted, and outputting it to the address storage means (detailed description, paragraph 44, Ito et al.);

said second overflow processing means comprises: a second comparison means for comparing the output of the addition means with the comparison reference value L X M-1; a second subtraction means for subtracting the comparison reference value L X M-1 from the output of the addition means; and a fifth selector for receiving the output of the addition means and the output of the second subtraction mean and selecting the output of the second subtraction means when the output of the addition means is equal to or

larger than the comparison reference value, arid selecting the output of the addition means when the output of the addition means is smaller than the comparison reference value; wherein the output of the fifth selector is supplied to the address storage means through the fourth selector during a period of time when the reset signal is not inputted (detailed description, paragraph 50, Ito et al.).

- As per claim 6, Ito et al. and Min teach the additional limitations.

Ito et al. teach the block interleaving apparatus, wherein the values of α and L X M-1 are set so that no common divisor exists between them (detailed description, paragraph 22, Ito et al.).

- As per claim 7, Ito et al. and Min teach the additional limitations.

Ito et al. teach the block interleaving apparatus, wherein the values of α and $M^{(-x)}$ are set so that α is not equal to $M^{(-x)}$, (detailed description, paragraph 21, Ito et al.).

- As per claim 8, Ito et al. and Min teach the additional limitations.

Ito et al. teach the block interleaving apparatus, wherein the values of α , L, and M are set at 20, 8, and 203, respectively (detailed description, paragraph 21-22, Ito et al.).

- As per claim 9, Ito et al. and Min teach the additional limitations.

Ito et al. teach the block interleaving apparatus, wherein the values of (L, M) are set at any of 72 possible values as follows:

L=96 x X (X=1, 2, 4), M=2, . . . , 13, or

M=2, . . . , 13, L = 96 x X (X=1, 2, 4) , (detailed description, paragraph 21-22, Ito et al.).

- As per claim 19, Ito et al. and Min teach the additional limitations.

Claim 19 (block interleaving method) follows the same limitations as claim 1 (block interleaving apparatus). See rejection to claim 1, above. Claim 19 is rejected under the same rational as to claim 1 rejected above.

- As per claim 20, Ito et al. and Min teach the additional limitations.

Claim 20 (block interleaving method) follows the same limitations as claim 4 (block interleaving apparatus). See rejection to claim 4, above. Claim 20 is rejected under the same rational as to claim 4 rejected above.

- As per claim 21, Ito et al. and Min teach the additional limitations.

Claim 21 (block interleaving method) follows the same limitations as claim 6 (block interleaving apparatus). See rejection to claim 6, above. Claim 21 is rejected under the same rational as to claim 6 rejected above.

- As per claim 22, Ito et al. and Min teach the additional limitations.

Claim 22 (block interleaving method) follows the same limitations as claim 7 (block interleaving apparatus). See rejection to claim 7, above. Claim 22 is rejected under the same rational as to claim 7 rejected above.

- As per claim 23, Ito et al. and Min teach the additional limitations.

Claim 23 (block interleaving method) follows the same limitations as claim 8 (block interleaving apparatus). See rejection to claim 8, above. Claim 23 is rejected under the same rational as to claim 8 rejected above.

- As per claim 24, Ito et al. and Min teach the additional limitations.

Claim 24 (block interleaving method) follows the same limitations as claim 9 (block interleaving apparatus). See rejection to claim 9, above. Claim 24 is rejected under the same rational as to claim 9 rejected above.

5. Claims 10-18, 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ito et al. (JP 2000078030 A) in view of Min (US 5,430,767) and Horii et al. (JP 2000036765 A).

As per claim 10, Ito et al. teach a storage means to which (L X M) pieces of addresses are allocated (L, M: integers, 2 <= L, M), (abstract, detailed description, paragraph 17, Ito et al.);

an address generation means for generating addresses for writing and reading blocks, each block having (L X M) pieces of data as a unit to be subjected to block interleaving in/from the storage means (abstract, Ito et al.);

said address generation means comprising: a multiplication means for generating the product of α (α: integer, 2<=) and $L^{(b-x)}$) (x: integer, 0<=x<=b, b: integer, 0<=b), every time a block of a block number b is

inputted (drawing 5, detailed description, paragraph 80-81, Ito et al.). The examiner would like to point out that in de-interleaving instead of M $^{(b-x)}$), L $^{(b-x)}$) is multiplied with α.

a first overflow processing means having a first comparison means for comparing the product obtained by the multiplication means with a comparison reference value L X M-1, and subtracting, as much as possible, the L X M-1 from the product on the basis of the comparison result to suppress overflow of the product, thereby outputting an address increment value REG corresponding to the block having the block number b (drawing 5, detailed description, paragraph 81-83, Ito et al.);

an addition means for successively adding the (n-1)th (n: integer, 1 <= n <= L X M-1) address Ab (n-1) of the block having the block number b, to the address increment value REG outputted from the first overflow processing means, every time the block of the block number b is inputted, thereby successively generating the n-th address Ab (n) in the block of the block number b (drawing 3, detailed description, paragraph 50, Ito et al.) ;

and a second overflow processing means having a second comparison means for comparing the sum obtained by the addition means with the comparison reference value L X M-1, and subtracting, as much as possible, the L X M-1 from the sum on the basis of the comparison result to suppress overflow of the sum, thereby outputting an address to be actually supplied to the storage means (detailed description, paragraph 50, Ito et al.) ;

wherein, when the first comparison means compares the product obtained by the multiplication with the comparison reference value L X M-1, the first comparison means employs, as a comparison reference value instead of the L X M-1, the minimum value A which exceeds the L X M-1 and is included in the product (detailed description, paragraph 81, Ito et al.).

However Ito et al. do not explicitly teach the specific use of a control means for controlling the storage means so that the storage means switches the operation between the data writing and the data reading, by using the addresses generated by the address generation means.

Min in an analogous art teaches that the switching operation is controlled by a memory controller for controlling read and write operations in the memory (col. 4, lines 13-15, Min).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ito et al.'s patent with the teachings of Min by including an additional step of using a control means for controlling the storage means so that the storage means switches the operation between the data writing and the data reading, by using the addresses generated by the address generation means.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a control means would provide the opportunity to interleave the data by writing and reading data in the memory.

Ito et al. also do not explicitly teach the specific use of a block deinterleaving apparatus.

However Horii et al. in an analogous art teach a deinterleaving circuit (abstract, Horii et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ito et al.'s patent with the teachings of Horii et al. by including an additional step of using a block deinterleaving apparatus.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using a block deinterleaving apparatus would provide the opportunity to retrieve the original data from the interleaved data and prevent burst errors.

- As per claim 11, Ito et al., Min and Horii et al. teach the additional limitations.

Ito et al. teach a storage means to which (L X M) pieces of addresses are allocated (L, M: integers, 2 <= L, M), (abstract, detailed description, paragraph 17, Ito et al.);

an address generation means for generating addresses for writing and reading blocks, each block having (L X M) pieces of data as a unit to be subjected to block interleaving, in/from the storage means (abstract, Ito et al.);

said address generation means including:

an address increment value storage means for storing an address increment value REG (b) corresponding to a block having a block number b (b: integer, 1 <= b), (detailed description, paragraph 17, Ito et al.);

a first initial value setting means for setting a (a: integer, 25) as an address increment value REG (0) corresponding to a block having a block number 0, in the address increment value storage means (detailed description, paragraph 17, Ito et al.);

a multiplication means for multiplying the output value REG (c) (c=b-1) from the address increment value storage means by L (detailed description, paragraph 17, Ito et al.). The examiner would like to point out that in de-interleaving instead of M (interleaving), the output value is multiplied by L.

Ito et al. teach a first overflow processing means having a first comparison means for comparing the product obtained by the multiplication means with a comparison reference value L X M-1, and subtracting, as much as possible, the L X M-1 from the product on the basis of the comparison result to perform a calculation equivalent to "α X L** (b-x) mod (LXM-1)" (L** (b-x) indicates $L^{(b-x)}$, mod is the remainder, x is an integer, 0 <= x <= b), thereby suppressing overflow, and outputting the calculation result as an address increment value REG(b) corresponding to the block of the block number b to the address increment value storage means (drawing 5, detailed description, paragraph 81-83, Ito et al.). The examiner would like to point out that in de-interleaving instead of M ** (b-x) (interleaving), L ** (b-x) is multiplied with α. The examiner would also like to point out that the calculation of "modulo" in claim 11 corresponds to the calculation of "comparison and subtraction" in the Ito et al. reference.

Ito et al. teach an address storage means for storing the n-th (n: integer, 1 <= n <= L X M-1) address Ab (n) in the block of the block number b, and outputting it to an address input terminal of the storage means (detailed description, paragraph 20, Ito et al.);

a second initial value setting means for setting the 0th address Ab (0) of the block of the block number b in the address storage means (detailed description, paragraph 21, Ito et al.);

an addition means for adding the address increment value REG (b) from the address increment value storage means to the output value Ab (p) (p=n-1) from the address storage means (detailed description, paragraph 22, Ito et al.);

a second overflow processing means having a second comparison means for comparing the sum obtained by the addition means with the comparison reference value L X M-1, and subtracting, as much as possible, the L X M-1 from the sum on the basis of the comparison result to perform a calculation

equivalent to " (Ab (n- X L**(b-x)) mod (L X M-1)", thereby suppressing overflow of the sum, and outputting the calculation result as the n-th address Ab (n) corresponding to the block having the block number b to the address storage means (detailed description, paragraph 50, Ito et al.);

wherein, when the first comparison means compares the product from the multiplication means with the comparison reference value L X M-1, the first comparison means employs, as a comparison reference value instead of the L X M-1, the minimum value A, which exceeds the L X M-1 and is included in the product (detailed description, paragraph 81, Ito et al.);

Min teaches a control means for controlling the storage means so that the storage means switches the operation between the data writing and the data reading, by using the addresses generated by the address generation means (col. 4, lines 13-15, Min).

Horii et al. teach a block deinterleaving apparatus (abstract, Horii et al.).

- As per claim 12, Ito et al., Min and Horii et al. teach the additional limitations.

Ito et al. teach that first initial value setting means comprises: a first: constant generation means for generating the α (detailed description, paragraph 34, Ito et al.); and a first selector for selecting the α from the first constant generation means when a reset signal is inputted, and outputting it to the address increment value storage means α (detailed description, paragraph 35, Ito et al.); said first overflow processing means comprises: a second selector for receiving the output of the multiplication means and the output of the address increment value storage means, and selecting the output of the multiplication means at the beginning of each block, and selecting the output of the address increment value storage means during a period of time other than the beginning of the block (detailed description, paragraph 80-83, Ito et al.);

a first comparison means for comparing the output of the second selector with the comparison reference value A; a first subtraction means for subtracting the L X M-1 from the output of the second selector (detailed description, paragraph 80-83, Ito et al.);

and a third selector for receiving the output of the second selector and the output of the first subtraction means, and selecting the output of the first subtraction means when the output of the second selector is equal to or larger than the comparison reference value, and selecting the output of the second selector

when the output of the second selector is smaller than the comparison reference value; wherein the output of the third selector is supplied to the address increment value storage means through the first selector during a period of time when the reset signal is not inputted (detailed description, paragraph 41, 50, 81, Ito et al.).

- As per claim 13, Ito et al., Min and Horii et al. teach the additional limitations.

Ito et al. teach that first comparison means employs, as a comparison reference value instead of the minimum value A exceeding the L X M-1, a value B, which satisfies L X M-1<B<A and is selected so that the number of logic gates constituting the comparison means is minimized (detailed description, paragraph 81, Ito et al.).

- As per claim 14, Ito et al., Min and Horii et al. teach the additional limitations.

Ito et al. teach that second initial value setting means comprises: a second constant generation means for generating a value 0 (detailed description, paragraph 18, Ito et al.);
and a fourth selector for selecting the value 0 from the second constant generation means when a reset signal is inputted, and outputting it to the address storage means (detailed description, paragraph 44, Ito et al.);
said second overflow processing means comprises: a second comparison means for comparing the output of the addition means with the comparison reference value L X M-1; a second subtraction means for subtracting the comparison reference value L X M-1 from the output of the addition means; and a fifth selector for receiving the output of the addition means and the output of the second subtraction means, and selecting the output of the second subtraction means when the output of the addition means is equal to or larger than the comparison reference value, and selecting the output of the addition means when the output of the addition means is smaller than the comparison reference value; wherein the output of the fifth selector is supplied to the address storage means through the fourth selector during a period of time when the reset signal is not inputted (detailed description, paragraph 50, Ito et al.).

- As per claim 15, Ito et al., Min and Horii et al. teach the additional limitations.

Ito et al. teach that the values of α and L X M-1 are set so that no common divisor exists between them (detailed description, paragraph 22, Ito et al.).

- As per claim 16, Ito et al., Min and Horii et al. teach the additional limitations.

Ito et al. teach that the values of α and $L^{(-x)}$ are set so that α is not equal to $L^{(-x)}$, (detailed description, paragraph 21, Ito et al.).

- As per claim 17, Ito et al., Min and Horii et al. teach the additional limitations.

Ito et al. teach that the values of α, L and M are set at 20, 8, and 203 respectively (detailed description, paragraph 21-22, Ito et al.).

- As per claim 18, Ito et al., Min and Horii et al. teach the additional limitations.

Ito et al. teach that the values of (L, M) are set at any of 72 possible values as follows:

L=96 x X (X=1, 2, 4), M=2, . . . , 13, or

M=2, . . . , 13, L = 96 x X (X=1, 2, 4) , (detailed description, paragraph 21-22, Ito et al.).

- As per claim 25, Ito et al., Min and Horii et al. teach the additional limitations.

Claim 25 (block deinterleaving method) follows the same limitations as claim 10 (block deinterleaving apparatus). See rejection to claim 10, above. Claim 25 is rejected under the same rational as to claim 10 rejected above.

- As per claim 26, Ito et al., Min and Horii et al. teach the additional limitations.

Claim 26 (block deinterleaving method) follows the same limitations as claim 13 (block deinterleaving apparatus). See rejection to claim 13, above. Claim 26 is rejected under the same rational as to claim 13 rejected above.

- As per claim 27, Ito et al., Min and Horii et al. teach the additional limitations.

Claim 27 (block deinterleaving method) follows the same limitations as claim 15 (block deinterleaving apparatus). See rejection to claim 15, above. Claim 27 is rejected under the same rational as to claim 15 rejected above.

- As per claim 28, Ito et al., Min and Horii et al. teach the additional limitations.

Claim 28 (block deinterleaving method) follows the same limitations as claim 16 (block deinterleaving apparatus). See rejection to claim 16, above. Claim 28 is rejected under the same rational as to claim 16 rejected above.

- As per claim 29, Ito et al., Min and Horii et al. teach the additional limitations.

Claim 29 (block deinterleaving method) follows the same limitations as claim 17 (block deinterleaving apparatus). See rejection to claim 17, above. Claim 29 is rejected under the same rational as to claim 17 rejected above.

- As per claim 30, Ito et al., Min and Horii et al. teach the additional limitations.

Claim 30 (block deinterleaving method) follows the same limitations as claim 18 (block deinterleaving apparatus). See rejection to claim 18, above. Claim 30 is rejected under the same rational as to claim 18 rejected above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 703-305-7853. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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